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7590 11/25/2009

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WASHINGTON,, DC 200373202

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/25/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,560	03/22/1999	TAKUMI HASEGAWA	Q53743	7269

TITLE OF INVENTION: DELAY ANALYSIS SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	02/25/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

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If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,560	03/22/1999	TAKUMI HASEGAWA	Q53743	7269

TITLE OF INVENTION: DELAY ANALYSIS SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	02/25/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
THANGAVELU, KANDASAMY	2123	703-002000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

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❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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Typed or printed name _____ Registration No. _____

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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/25/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	KANDASAMY THANGAVELU	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *August 24, 2009*.

2. ☒ The allowed claim(s) is/are *1-4*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean Copy of Allowed Claims*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Appeal Brief filed on August 24, 2009. Claims 1-6 of the application are pending.

Examiner's Amendment

2. An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Quadeer Ahmed on November 20, 2009.

3. The application has been amended as follows:

In the claims:

Replace claim 1-4 with:

1. A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said delay analysis system comprising:

a delay analysis library comprising:

connection information and delay time information on rises and falls of input and output terminals for a plurality of circuits; and

for at least one circuit of said plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

a delay analyzing module which computes delay times of the plurality of the circuits based on information in the delay analysis library,

wherein delay time for a signal path from input terminals to an output terminal of a logical circuit of said at least one circuit is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal of a logical circuit is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

selecting the delay time from the input terminals to the output terminal of the logical circuit from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition

triggers said high state to said low state transition at said selected output terminal according to the logical operation information,

wherein the delay analyzing module automatically computes the delay of the logical circuit based on the delay time information and the logical operation information in said delay analysis library.

2. A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said system comprising:

a delay analysis library comprising:

connection information and delay time information on rises and falls of input and output terminals for a plurality of circuits; and

for each of said plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

a delay analyzing module which computes delay times of the plurality of the circuits based on information in the delay analysis library,

wherein, respective delay time for a signal path from input terminals to an output terminal of a respective logical circuit of each of said plurality of circuits is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the respective logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal of the respective logical circuit is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

selecting the delay time from the input terminals to the output terminal of the respective logical circuit from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information,

wherein the delay analyzing module automatically computes the delay of the respective logical circuit of each of said plurality of circuits based on the respective delay time information and the logical operation information in said delay analysis library.

3. A computer-implemented method of making a delay analysis of a logical circuit, comprising:

referencing, using a computer, a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising:

connection information, delay time information on rises and falls of input and output terminals for said plurality of circuits; and

for the at least one circuit among the plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

computing by a delay analyzing module delay times for the at least one circuit of the plurality of the circuits based on information in the delay analysis library,

wherein, delay time for a signal path from input terminals to an output terminal for the at least one circuit among a plurality of circuits is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal for the at least one circuit among a plurality of circuits is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

automatically selecting a delay time from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information.

4. A computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

referencing a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising:

connection information, delay time information on rises and falls of input and output terminals for said plurality of circuits; and

for the at least one circuit among the plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

computing by a delay analyzing module delay times for the at least one circuit of the plurality of the circuits based on information in the delay analysis library,

wherein, delay time for a signal path from input terminals to an output terminal for the at least one circuit among a plurality of circuits is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal for the at least one circuit among a plurality of circuits is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

automatically selecting a delay time from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information.

Cancel Claims 5 and 6.

A clean copy of the allowed claims is attached.

Reasons for Allowance

4. Claims 1-4 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a high speed delay analysis apparatus and method that includes tracing a circuit based on the circuit information stored in a delay model storage device, to shorten the delay verification time; the circuit information stored includes logic information, connection

information and delay information of the logic circuit; a tracing device calculates for each pin of the logic circuit, a delay time from each pin to the starting point within the logic circuit and a delay time from each pin to the ending point within the logic circuit based on the contents of the delay model storage device; the tracing device obtains the maximum value of the delay for each node; the tracing device adds the maximum value of the delay time to the circuit information of the delay model storage device stores it to an additional model storing device; a limit inspecting device deletes, based on the information stored in the additional model storing device, the node and its arc in which the sum of maximum value of delay time is less a preset limit and stores such node and arc information in a modified model storage device; the limit inspecting device may also delete, based on the information stored in the additional model storing device, the node and its arc in which the sum of the minimum value of the delay time is greater than a second limit value and then store such node and arc information in the modified model storage device; a delay verification device verifies the delay based on the circuit information of the modified model storing device; high speed delay verification is achieved by calculating the delay time from each pin to the starting point of the logic circuit and the delay time from each pin to the ending point of the logic circuit based on the information of the logic circuit such as logic information, connecting information and delay information; thereafter, delay verification is performed on the circuit by verifying each node based on the information of the circuit model, and deleting nodes for which the sum delay up to the starting point and the sum delay up to the ending point is less than the preset limit (**Hasegawa,** U.S. Patent 6,041,168);

(2) a delay time verifier to verify the delay time for a logic circuit using a delay time verification model that is based on graph theory; when the logic circuit is expressed as a

validness graph according to certain rules various processing regarding the characteristics of the circuit can be made easily; the arcs have directions corresponding to the flow of signals; the delay time is provided for each rise or fall type for the start point and end point nodes of every arc; the weight of an arc is the delay time for each rise/fall type of the start point and end point nodes; the delay time verification method provides correct delay time, even when either rise or fall of the signal is meaningless in a delay time verification process; the model stores in advance the delay time verification information for each of the arcs in the time verification model; the stored information includes the delay time for each rise/fall type signal at the start point node and the end point node of the arc, an invalidness specifier to specify an arc with invalid data and rise or fall of the signal to be invalidated for the arcs where only one of the rise and fall signals is to be allowed to be valid; a modifier modifies the delay time verification information stored in the file, so the information for the arcs whose rise or fall signal specified by the invalidness specifier becomes invalid is modified; the delay time verifier verifies the delay time of the logic circuit based on the delay time verification information after modification by the modifier (**Hasegawa,** U.S. Patent 5,528,511); and

(3) a method of emulating the delay time associated with individual cells and integrated array of cells such as those in ASIC, including cell libraries; the method provides a more accurate estimate of the actual delay times than available in prior methods; the emulation comprises determining an edge delay base factor which approximates the delay time of at least the rising edge or the falling edge of a signal through the cell; calculating an edge delay correction factor based substantially on the slew rate of the signal applied to at least one input pin of the cell; adding the edge delay base factor to the corresponding edge delay correction

factor; approximating the delay time of an excitation through a logic cell using the summation of a base delay, which is a function of the delay coefficients for the cell and total output capacitance of the cell and a rise/fall correction which is determined from the output rise/fall time of the driving cell; the emulation program uses coefficients from the database as input to the algorithms and estimates the cell delay time; the cell delay time and other delay times for the circuit are used to verify the circuit performance for specified input/output conditions (**Blinne et al.,** U.S. Patent 5,274,568).

None of these references taken either alone or in combination with the prior art of record discloses a delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, specifically including:

(Claim 1) "for at least one circuit of said plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

a delay analyzing module which computes delay times of the plurality of the circuits based on information in the delay analysis library,

wherein delay time for a signal path from input terminals to an output terminal of a logical circuit of said at least one circuit is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal of a logical circuit is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

selecting the delay time from the input terminals to the output terminal of the logical circuit from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information" in combination with the remaining elements and features of the claimed invention.

None of these references taken either alone or in combination with the prior art of record discloses a delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, specifically including:

(Claim 2) "for each of said plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

a delay analyzing module which computes delay times of the plurality of the circuits based on information in the delay analysis library,

wherein, respective delay time for a signal path from input terminals to an output terminal of a respective logical circuit of each of said plurality of circuits is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the respective logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal of the respective logical circuit is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

selecting the delay time from the input terminals to the output terminal of the respective logical circuit from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information" in combination with the remaining elements and features of the claimed invention.

None of these references taken either alone or in combination with the prior art of record discloses a computer-implemented method and a computer-readable medium having stored

thereon a program comprising computer instructions that, when executed on a computer, perform a process of making delay analysis of a logical circuit, specifically including:

(Claims 3 and 4) "for the at least one circuit among the plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

computing by a delay analyzing module delay times for the at least one circuit of the plurality of the circuits based on information in the delay analysis library,

wherein, delay time for a signal path from input terminals to an output terminal for the at least one circuit among a plurality of circuits is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal for the at least one circuit among a plurality of circuits is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

automatically selecting a delay time from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said

selected output terminal according to the logical operation information" in combination with the remaining elements and features of the claimed invention.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
November 20, 2009

/Paul L Rodriguez/
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